[0053] **FIG. 4** is a timing chart schematically showing an example of a method of driving the display shown in FIGS. **1** to **3**. **FIG. 4** illustrates a driving method in the case that the number of rows which the pixels form is M. In the figure, the abscissa indicates time, while the ordinate indicates potential.

[0054] As for the "XDR output" in **FIG. 4**, during the period shown as "$I_{sig}(m)$", the video signal line driver XDR outputs a video signal $I_{sig}(m)$ to the video signal line DL. During the period shown as "V_{rst}", the video signal line driver XDR outputs a reset signal V_{rst} to the video signal line DL. In **FIG. 4**, the waveforms shown as "SL1 potential" and "SL2 potential" represent the potentials of the scan signal lines SL1 and SL2, respectively. In **FIG. 4**, the waveform shown as "CL potential" represents the potential of the control signal line CL.

[0055] According to this method, an effective scanning period and a blanking period are repeated alternately. During the effective scanning period, rows of the pixels are sequentially selected while the switch SW_{vs} is opened. A write operation is executed on each pixel included in a selected row. A display operation is executed on each pixel included in non-selected rows.

[0056] For example, during a period that a m-th row of pixels is selected (to be referred to as m-th row selection period), the switch SWa of each pixel included in the m-th row is opened. Then, the multiplexer MLT outputs 6-bit digital video signal to each current source CS, and the switches SWb and SWc of each pixel included in the m-th row are closed.

[0057] The current source CS converts the digital video signal into a write current $I_{sig}m$ as an analog video signal. The write current $I_{sig}m$ flows from the first power supply terminal ND1 to the current source CS. As a result, the gate potential of the drive control element DR is set at a value when the write current $I_{sig}m$ flows between the source and drain of the drive control element DR.

[0058] Thereafter the switches SWb and SWc are opened. Then, the switch SWa is closed to finish the m-th row selection period.

[0059] When the switch SWa is closed, a drive current $I_{drv}m$ whose magnitude corresponds to a magnitude of the write current $I_{sig}m$ flows through the organic EL element OLED. During the non-selection period, the switch SWa is kept closed. Therefore, the organic EL element OLED of each pixel PX continues light-emission at a luminance corresponding to the magnitude of the drive current $I_{drv}m$ until the pixel is selected again.

[0060] During a blanking period, a reset operation is executed. Firstly, all the switches SW_{dgt} are opened. Then, the switch SW_{vs} is closed, and the voltage source VS outputs a reset signal to the video signal line DL. That is, the potential of the video signal line DL is set at a reset potential. Subsequently, the switch SW_{vs} is opened. Note that, during the blanking period, the switches SWb and SWc are kept open in all the pixels PX.

[0061] Given that the video signal line driver XDR of the display does not include the voltage source VS and the switch SW_{vs}, the video signal line DL can be considered to be in floating state during the blanking period. However, a small reverse current, i.e., a leakage current, flows through each of the diodes D1*a*, D1*b*, D2*a*, and D2*b*. The sum of the leakage currents flowing through the diodes D1*a* and D2*a* is not necessarily equal to the sum of the leakage current flowing through the diodes D1*b* and D2*b*.

[0062] For this reason, the potential of the video signal line DL just after the blanking period ends may differ from the potential of the video signal line DL just after stating the blanking period. For example, the potential of the video signal line DL just after the blanking period ends may be lower than the lowest potential of the video signal line DL to be set by the write operation.

[0063] In this case, in order to display a gray level within a low gray level range on a pixel PX in the 1st row, the potential of the video signal line DL must be greatly increased by the write operation during the 1st row selection period. However, since a magnitude of the write current $I_{sig}1$ for displaying a gray level within the low gray level range is small, it is difficult to sufficiently change the potential of the video signal line DL during the 1st row selection period. Thus, for the pixel in the 1st row, the gate potential of the drive control element DR cannot be accurately set at a value corresponding to a magnitude of the write current $I_{sig}1$, and this makes it difficult to display each gray level within the low gray level range with a high reproducibility.

[0064] When the potential of the video signal line DL greatly changes during the blanking period, a similar phenomenon occurs in the pixels PX included in several rows encountered after the active scanning period has started. It is thus conventionally difficult for the pixels PX in several rows first selected during the active scanning period to display gray levels in the low gray level range with a high reproducibility.

[0065] In contrast, by executing the reset operation described with reference to FIGS. **1** to **4** during the blanking period, the potential of the video signal line DL just before starting the write operation on the pixels PX in the 1st row can be set almost equal to the reset potential. Consequently, by setting the reset signal at a value almost equal to the potential of the video signal line DL to be set by the write operation when the video signal $I_{sig}m$ corresponds to the lowest gray level for example, it becomes possible to greatly decrease an amount of change in the potential of the video signal line necessary for displaying a gray level within the low gray level range on the pixels PX in the 1st row. Therefore, it is possible for the pixels PX in several rows first selected during the active scanning period to display gray levels in the low gray level range with a high reproducibility.

[0066] The magnitude of the reset signal may be differ from the potential of the video signal line DL to be set by the write operation when the video signal $I_{sig}m$ corresponds to the lowest gray level. The magnitude of the reset signal may be set at a voltage within a voltage range of the video signal line that the write operation can set. In view of displaying each gray level in the low gray level range with a high reproducibility, it is advantageous that the magnitude of the reset signal is almost equal to the voltage of the video signal line DL to be set by the write operation when the video signal corresponds to the lowest gray level.

[0067] A second embodiment of the present invention will be described below.